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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,732	02/27/2004	Chenghung Justin Chen	200400184-1	8404

22879 7590 09/25/2007  
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FORT COLLINS, CO 80527-2400

EXAMINER
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FAHERTY, COREY S

ART UNIT	PAPER NUMBER
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2183

MAIL DATE	DELIVERY MODE
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09/25/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/789,732	CHEN ET AL.
	Examiner	Art Unit
	Corey S. Faherty	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 27 February 2004.

2a) This action is FINAL.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-29 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_.

**DETAILED ACTION**

1. This office action is in response to the application filed on 02/27/2004.
2. Claims 1-29 are pending in the application and have been examined.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 6-10 and 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Claims 6 and 17 recite the limitation “said instruction”. There is insufficient antecedent basis for this limitation in the claims.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson et al. (*Cyclical Cascade Chains: A Dynamic Barrier Synchronization Mechanism for Multiprocessor Systems*), referenced from here forward as Johnson.

8. Regarding claims 1 and 12, Johnson discloses a method for synchronizing a plurality of processors of a multi-processor computer system on a synchronization point [page 1, abstract], comprising: triggering a first set of processors, using a lead processor of said plurality of processors when said lead processor encounters said synchronization point, to enter an exit holding loop [page 6, section 6; a processor calls a *wait* routine when it reaches a barrier to indicate to other processors that a barrier must be completed], said first set of processors representing said plurality of processors except said lead processor, said triggering said first set of processors being performed without accessing a shared memory area of said multi-processor system [page 6, section 6; no shared memory is used in the triggering]; and triggering said plurality of processors, using a tail processor of said plurality of processors when said tail processor encounters said synchronization point, to leave said exit holding loop [page 4, first column, second paragraph; sections 4 and 5; a barrier is completed when all processors assigned to that barrier have reached the barrier; the processors communicate as a circular linked list so that, when the final processor reaches the barrier, execution can continue; page 4, section 4, paragraph 1; a processor will only indicate that it can proceed when it has reached the barrier and the processor immediately above it can proceed], said triggering said plurality of processors being performed without accessing said shared memory area of said multi-processor system [sections 4 and 5; no shared memory is used in the triggering].

9. Regarding claims 2 and 13, Johnson discloses the method of claim 1 further comprising creating a circular reference arrangement for said plurality of processors [page 4, first column, second paragraph; the processors are arranged as a cyclical doubly linked list], one of said plurality of processors being designated said lead processor, another one of said processors being

designated said tail processor, said lead processor being adjacent to said tail processor in said circular reference arrangement [page 4, Figure 5; the system contains four processors, each cyclically connected to two others; page 6, section 6; the lead processor executes a *wait* routine; the processor that is above the lead processor is the tail processor].

10. Regarding claims 3, 14 and 24, Johnson discloses the method of claim 2 wherein said circular reference arrangement represents a circular linked list [page 4, first column, second paragraph; the processors are arranged as a cyclical doubly linked list].

11. Regarding claims 4 and 15, Johnson discloses the method of claim 2 wherein said triggering said first set of processors is performed in a cascading manner starting with said lead processor following a sequence established by said circular reference arrangement, with each processor of said first set of processors being triggered by its immediate predecessor in said sequence [page 4, first column, second and third paragraphs; Figure 5; sections 4 and 5; the processors are connected in a circular fashion so that each indicates to another when it is ready to proceed beyond the barrier].

12. Regarding claims 5 and 16, Johnson discloses the method of claim 4 wherein said triggering said plurality of processors is performed in a cascading manner starting with said tail processor following said sequence established by said circular reference arrangement, with each processor of said plurality of processors being triggered by its immediate predecessor in said sequence [page 4, first column, second and third paragraphs; Figure 5; sections 4 and 5; the processors are connected in a circular fashion so that each indicates to another when it is ready to proceed beyond the barrier].

13. Regarding claims 6, 17 and 23, Johnson discloses the method of claim 5 further comprising enabling processors of said first set of processors to enter an entry holding loop if said processors of said first set of processors encounter said instruction before said lead processor [page 4, section 4, paragraph 1; sections 4 and 5; when a processor encounters a barrier point, the processor waits until all other processors associated with that barrier have reached the barrier point].

14. Regarding claims 7, 18 and 25, Johnson discloses the method of claim 6 wherein said triggering said first set of processors employs a first external interrupt mechanism associated with each of said first set of processors [page 6, first column, second full paragraph; the signals used to indicate that a processor has reached a barrier are externally input].

15. Regarding claims 8, 19 and 26, Johnson discloses the method of claim 7 wherein said triggering said first set of processors includes writing to hard physical addresses of each of said first set of processors [page 6, first column, last paragraph, second column, first full paragraph; a processor specifies the processor in which it will write its *SendTo* signal].

16. Regarding claims 9, 20 and 27, Johnson discloses the method of claim 6 wherein said triggering said plurality of processors employs a second external interrupt mechanism associated with each of said plurality of processors [page 6, first column, second full paragraph; the signals used to indicate that a processor has reached a barrier are externally output].

17. Regarding claims 10, 21 and 28, Johnson discloses the method of claim 9 wherein said triggering said plurality of processors includes writing to hard physical addresses of each of said plurality of processors [page 6, first column, last paragraph, second column, first full paragraph; a processor specifies the processor in which it will write its *SendTo* signal].

18. Regarding claims 11, 22 and 29, Johnson discloses the method of claim 1 wherein said triggering said first set of processors employs a masked interrupt approach [page 6, section 6; a masking technique is used to determine which processors will be interrupted by the barrier].

***Conclusion***

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references are closely related to the subject matter of the instant application and should be fully considered in any reply to this office action.

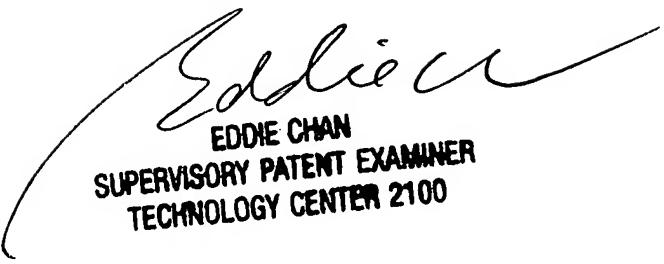
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Corey S Faherty  
Examiner  
Art Unit 2183

CF



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